WHAT IS CLAIMED IS:

1. A simulation coverage calculating apparatus for calculating a simulation coverage for a logic circuit, comprising:

a first input unit reading a property that represents one or more effective test patterns to the logic circuit to be verified;

an effective test pattern calculating unit calculating the effective test patterns based on the property;

a second input unit reading one or more test patterns entered and executed by a verifier;

a coverage ratio calculating unit calculating a coverage ratio from a ratio of the number of the test patterns matched to the effective test patterns to the number of all of the effective test patterns; and

an output unit outputting the calculated coverage ratio.

2. The simulation coverage calculating apparatus according to claim 1, wherein the property represents the effective test patterns with the combinations of signals and the time information.

3. A simulation coverage calculating method for calculating a simulation coverage for a logic circuit

through the use of a computer, comprising the steps of:

reading a property that represents one or more effective test patterns to the logic circuit to be verified;

calculating the effective test patterns based on the property;

reading one or more test patterns entered and executed by a verifier; and

calculating a coverage ratio from a ratio of the number of the test patterns matched to the effective test patterns to the number of all of the effective test patterns.

4. The simulation coverage calculating method according to claim 3, wherein the property represents the effective test patterns with the combinations of signals and the time information.